ALU TESTBENCH

module alu\_tb;

// Inputs

reg [31:0] a, b;

reg [2:0] alucont;

// Outputs

wire [31:0] result;

wire zero;

// Instantiate the ALU

alu uut (

.a(a),

.b(b),

.alucont(alucont),

.result(result),

.zero(zero)

);

// Stimulus

initial begin

$display("Testing ALU Operations");

// Test 1: ADD

a = 5;

b = 10;

alucont = 3'b010; // ADD

#10;

if (result !== a + b || zero !== 0) $display("Test 1 Failed");

// Test 2: SUB

a = 15;

b = 8;

alucont = 3'b110; // SUB

#10;

if (result !== a - b || zero !== 0) $display("Test 2 Failed");

// Test 3: AND

a = 8;

b = 12;

alucont = 3'b000; // AND

#10;

if (result !== (a & b) || zero !== 0) $display("Test 3 Failed");

// Test 4: OR

a = 3;

b = 5;

alucont = 3'b001; // OR

#10;

if (result !== (a | b) || zero !== 0) $display("Test 4 Failed");

// Test 5: SLT

a = 8;

b = 12;

alucont = 3'b111; // SLT

#10;

if (result !== 1 || zero !== 0) $display("Test 5 Failed");

$stop;

end

endmodule